4-7. Self Test Acquisition Test Procedure

PURPOSE:

This test verifies the processor's ability to configure the system to take a state measurement. It also verifies that all pod channels can sample data between -9.9 and +9.9 volts.

CIRCUITRY TESTED:

This test checks the processor, system timing control, state and timing boards, and the pods.

OPERATION:

a. Both RAM and ROM tests must have passed before this test begins.

b. The processor configures the system for a Trace Specification of <don't care start-on any state, trace all states>.

c. System starts tracing with pods 4, 2, 0 thresholds set at +9.9 volts and pods 3 and 1 set at -9.9 volts. "0s" should be sampled on pods 4, 2, 0 and "1s" should be sampled on pods 3 and 1.

d. 512 states are clocked in and sampled at this threshold pattern.

e. A sample is taken for "measurement complete". It should be false.

f. The pod threshold voltages are reversed, making the sample pattern of step (c) reversed.

g. 511 states are clocked in and sampled at this threshold pattern.

h. A sample is taken for "measurement complete". It should be false.

i. The memory counter is sampled for words remaining; one should remain.

j. The last word is clocked in, making the "measurement complete" status true. The trace is then halted.

k. Any acquisition errors are summarized and the self test determines if a Timing Slave board is in the instrument. If a Timing Slave board is not in the system, errors are ignored for the Timing Slave channels.

l. If an error occurred, a "Acq Error XX . . . XX" message will be displayed in hex. The number of hex pairs in the message depends on the instrument model. See the error message information following.

m. If no errors occurred "Self Test Passed Reset Rear Panel Switch to xxxx x0xx to continue" message should be displayed. When the switch is reset the System Specification menu should be displayed.

ERROR MESSAGE INTERPRETATION

There are two forms of acquisition error message in the HP 163X family.

```
"Acq error XX XX XX XX XX XX XX XX XX XX"
```

This error message is present on the latest versions of the HP 163X family and can be generally thought of as covering instruments with disc-based mass storage capability. This message must be interpreted differently depending on whether the instrument is a 1630/31A/D or a 1630G. Table 4-1 covers specific interpretation of 1630/31A/D messages and table 4-2 covers 1630G messages.

```
"Acq error XX XX XX XX XX XX XX"
```

This message covers earlier versions of HP 1630A/D and all 1630A/D option 007. These instruments have firmware for using them with tape-based mass storage. Specific interpretation of error messages is covered in table 4-3.

The error message, a series of HEX digits must be converted to a binary equivalent before it can be fully interpreted. The following general example of a 1631D failure shows how this is done.

```
"Acq error 01 80 00 00 00 00 03 00 00 00"

   01       80       00       00       00       00       03       00       00       00
00000001 10000000 00000000 00000000 00000000 00000000 00000011 00000000 00000000 00000000
```

a. This example shows that incorrect Acquisition data was acquired.

b. Trace point was not found.

c. All channels passed except pod 0 (Timing Master) Channels 1 and 0.

d. All analog acquisition passed.

If failures occur in this test, try swapping LIKE pods to determine if the problem follows the pod. If the failure does follow the pod, that pod may need to be replaced.

Whenever an acquisition error occurs, always check that the pods are properly seated in their connectors and that none of the connector pins are bent. If all of the channels on any board fail, check that the board is properly seated in it's motherboard connector.

After completion of the self-test, continue with the operational tests (see chart on page A-2 for 1630/31A/D or page A-4 for 1630G).

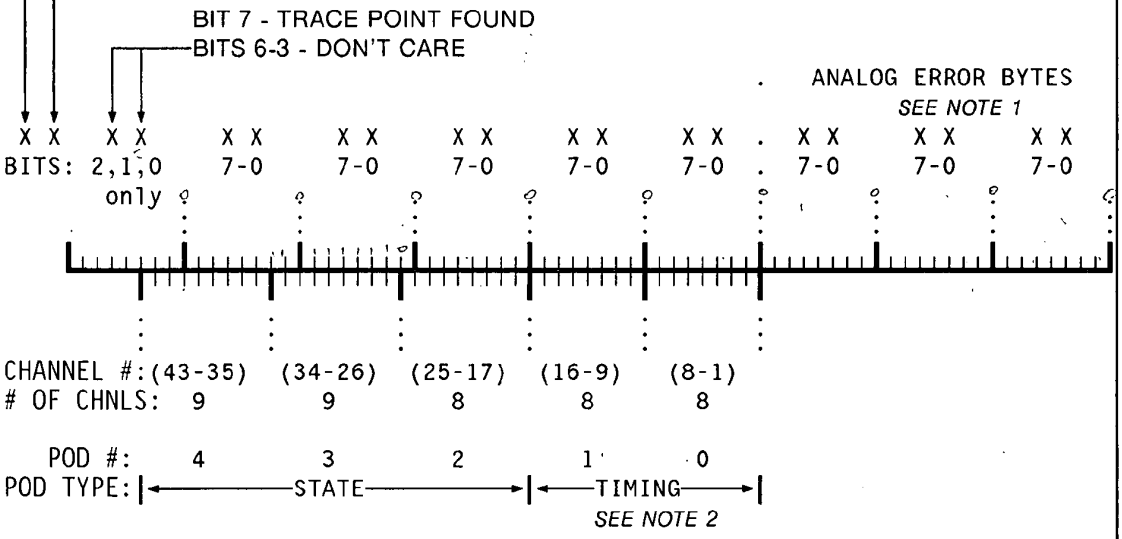
Table 4-1. 1630A/D, 1631A/D Error Mesage Interpretation.

This table covers interpretation of errors in 1630A/D and 1631A/D in the most recent versions, those with disc-based mass-storage capability.

For earlier 1630A/D, those with tape-based mass storage (also option 007), see table 4-3.

KEY 1 = Error (except Don't Cares)
0 = No Error

Bit 0 - Incorrect acquisition data acquired.
Bit 1 - "Measurement Complete" true when it should be false.
Bit 2 - "Measurement Complete" IRQ true when it should be false.
Bit 3 - Words remaining. State Master board counter incorrect.
Bit 4 - "Measurement complete" on State Master board false when it should be true.
Bit 5 - "Measurement complete" false when it should be true, no "interrupt" received.
Bit 6,7 - Don't Care Bits



NOTE 1: Analog errors are only relevant in the 1631A/D. For 1630A/D this section of the error code will show all bits passing. For analog errors see paragraph 4-8.

NOTE 2: In the case of timing errors, channels 8-1 actually represent the Timing Master and channels 16-9 the Timing Slave. The example above represents a 1630/31D. If the instrument is a 1630/31A, the test will show channels 16-9 as passing and channels 8-1 will represent POD 1.

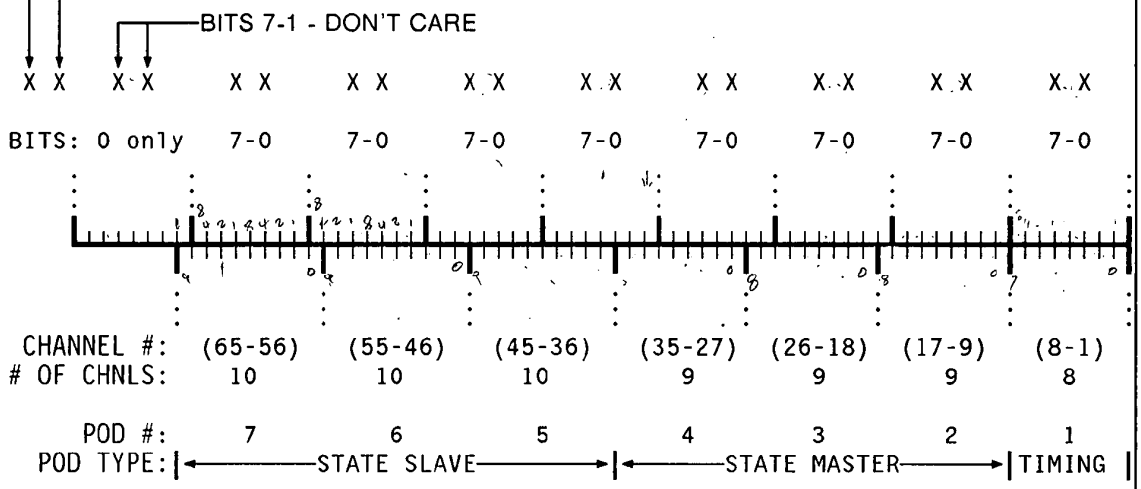
NOTE 3: Each pair of analog error bytes has 8 bits (4 bits per byte). Since the timing pods (pods 0 and 1) have 8 channels, the 8-bit pairs of error bytes interpret directly to the timing pods' 8 channels. However, the state pods (pods 2, 3, 4) have 9 channels, and the byte to channel interpretation is offset by one bit per pod. As in the diagram above, the one bit offset must be taken into account when interpreting acquisition errors.

Table 4-2. 1630G Error Mesage Interpretation.

This table covers error message interpretation in 1630G only.

KEY 1 = Error (except Don't Cares)
0 = No Error

Bit 0 - Incorrect acquisition data acquired.
Bit 1 - "Measurement Complete" true when it should be false.
Bit 2 - "Measurement Complete" IRQ true when it should be false.
Bit 3 - Words remaining. State Master board counter incorrect.
Bit 4 - "Measurement complete" on State Master board false when it should be true.
Bit 5 - "Measurement complete" false when it should be true, no "interrupt" received.
Bit 6,7 - Don't Care Bits



NOTE: Since the timing pod has 8 channels, the 8-bit pair of error bytes interpret directly to the timing pods' 8 channels. However, the state master pods (pods 2, 3, 4) have 9 channels, and the byte to channel interpretation is offset by one bit per pod. The State Slave pods (pods 5, 6, and 7) have 10 channels and the byte to channel interpretation is offset by two bits per pod. As in the diagram above, the bit offset must be taken into account when interpreting acquisition errors.

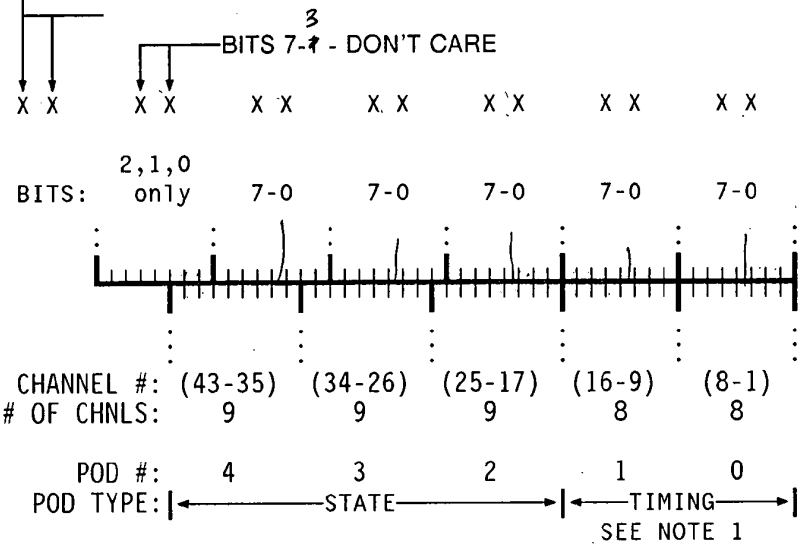
Table 4-3. Earlier 1630A/D Error Mesage Interpretation.

This table covers error message interpretation in 1630A/D of earlier vintage as well as recent 1630A/D with tape-based mass-storage (option 007).

For recent 1630A/D, those using disc-based mass-storage, see table 4-1.

KEY 1 = Error (except Don't Cares)
0 = No Error

Bit 0 - Incorrect acquisition data acquired.
Bit 1 - "Measurement Complete" true when it should be false.
Bit 2 - "Measurement Complete" IRQ true when it should be false.
Bit 3 - Words remaining. State Master board counter incorrect.
Bit 4 - "Measurement complete" on State Master board false when it should be true.
Bit 5 - "Measurement complete" false when it should be true, no "interrupt" received.
Bit 6,7 - Don't Care Bits



NOTE 1: In the case of timing errors, channels 8-1 actually represent the Timing Master and channels 16-9 the Timing Slave. The example above represents a 1630D. If the instrument is a 1630A, the test will show channels 16-9 as passing and channels 8-1 will represent POD 1.

NOTE 2: Since the timing pod has 8 channels, the 8-bit pair of error bytes interpret directly to the timing pods' 8 channels. However, the state pods (pods 2, 3, 4) have 9 channels, and the byte to channel interpretation is offset by one bit per pod. As in the diagram above, the bit offset must be taken into account when interpreting acquisition errors.